

ABSTRACT

A line selector for a matrix of memory elements, for example a word line selector, comprises a plurality of line group selection circuits, each one allowing the
5 selection of a respective group of matrix lines according to an address; each matrix line group includes at least one matrix line. Flag means are associated with each line group, that can be set to declare a pending status of a prescribed operation, for example an erase operation, for the respective matrix line group. Means are
provided for entrusting the flag means with the selection of the respective line group
10 during the execution of the prescribed operation, in alternative to the respective line group selection circuit. The flag means enable, when set, the execution of the prescribed operation on the respective matrix line group.